CCD261-84 Scientific CCD Sensor
Back Illuminated, 2048 x 4096 Pixels, Non Inverted Mode Operation
Enhanced red sensitivity

INTRODUCTION

This device is primarily a full-frame sensor with an image area of 2048 x 4104 pixels, but dual connections are provided for the option of frame-transfer operation. Back illumination technology, in combination with an extremely low noise amplifier, makes the device well suited to the most demanding applications, such as astronomy.

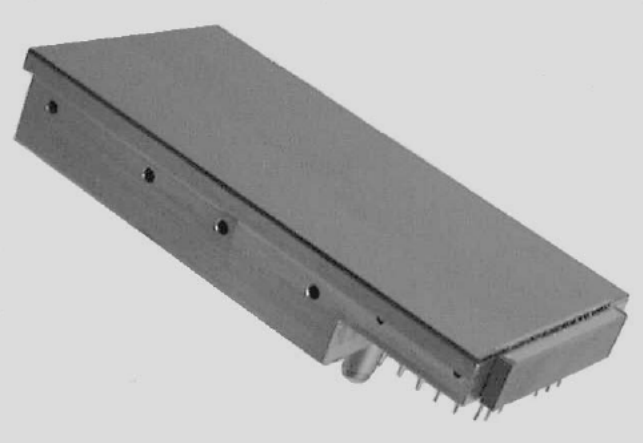
The new 'high-rho' technology is used to increase the thickness of the silicon to maximise the response at the infra-red end of the spectral range. The device operates in the same manner as other e2v sensors, but with additional guard-drain and back-substrate bias voltages to fully deplete the silicon. Details are given at the end of this datasheet. Devices of different thickness are to be available ranging from 100 µm to 300 µm.

The output amplifier is designed to give low noise at pixel rates as high as 1 MHz and the low output impedance and optional JFET buffer simplify the interface with external electronics.

The device is supplied in a package designed to facilitate the assembly of large close-butted mosaics used at cryogenic temperatures. The design of the package ensures that the device flatness is maintained at the working temperature.

The sensor is shipped in a protective container, but no permanent window is fitted.

Other variants and formats can be provided; please consult the factory.



SUMMARY SPECIFICATION (Typical values; TBC)

Number of pixels	2048(H) x 4104(V)
Pixel size	15 µm square
Image area	30.7 mm x 61.6 mm
Outputs	2
Package size	31.8 mm x 66.4 mm
Package format	Buttable Invar metal package with PGA connector
Focal plane height, above base	14.0 mm
Connectors	40-pin PGA
Flatness	20 µm p-v
Amplifier responsivity	7.5 µV/e^-
Readout noise	2.5 e^- at 100 kHz
Maximum data rate	1 MHz
Image pixel charge storage	200,000 e^-
Dark signal	0.1 e^-/pixel/hr (153K)

The performance parameters shown here are "typical" values. Specification limits are given on the following pages.

Part References

CCD261-84-g-xxx
g = cosmetic grade

xxx= specific variant type (eg thickness and AR coating)

CCD261-84-g-E65
Basic NIR response

CCD261-84-g-E77
Astro multi-2 response

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PERFORMANCE (at 173 K unless stated)

Electro-Optical Specification

	Min	Typical	Max	Units	Notes
Peak charge storage (image)	150,000	200,000	-	e^-/pixel	1
Peak charge storage (register)	-	500,000	-	e^-/pixel	
Output node capacity	-	300,000	-	e^-	
Output amplifier responsivity	7	7.5	-	$\mu V/e^-$	2
Read-out noise	-	2.5	4	e^- rms	3
Read-out frequency	-	100	1000	kHz	4
Dark signal at 153K	-	0.1	2.0	e^-/pixel/h	5
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9995 99.9998	 - -	 % %	6

NOTES

Note 1. Signal level at which resolution begins to degrade.

Note 2. Responsivity increases by approximately 5% as BSS changes from 0V to -70V.

Note 3. Measured with correlated double sampling at 100 kHz pixel rate.

Note 4. Depending on the external load capacitance to be driven. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.

Note 5. Dark signal is typically measured at 173 K. It is a strong function of temperature and the typical average (background) dark signal is taken as:

$$Q_D/Q_{DO} = 122T^3e^{-6400/T}$$

where Q_{DO} is the dark current at 293 K.

Note 6. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

Cosmetic quality and spectral response are specified on the following pages.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Grade	0	1	2	(Grade-1 typical)
Column defects: (black or white)	4	10	20	TBD
White spots	500	1000	2000	TBD
Total spots (black and white)	100	2000	4000	TBD
Traps > 200e-	20	30	50	TBD

There is some dependence on VBSS; indications are that defect count increases for highest values of VBSS. This is associated with device thickness; see note below QE section also. Specification levels apply with VBSS= -50V.

It should be noted that this device type can exhibit some “roll off “ of sensitivity of the columns at each edge of the device; image columns 1,2 and 2047, 2048 are excluded from cosmetic specification.

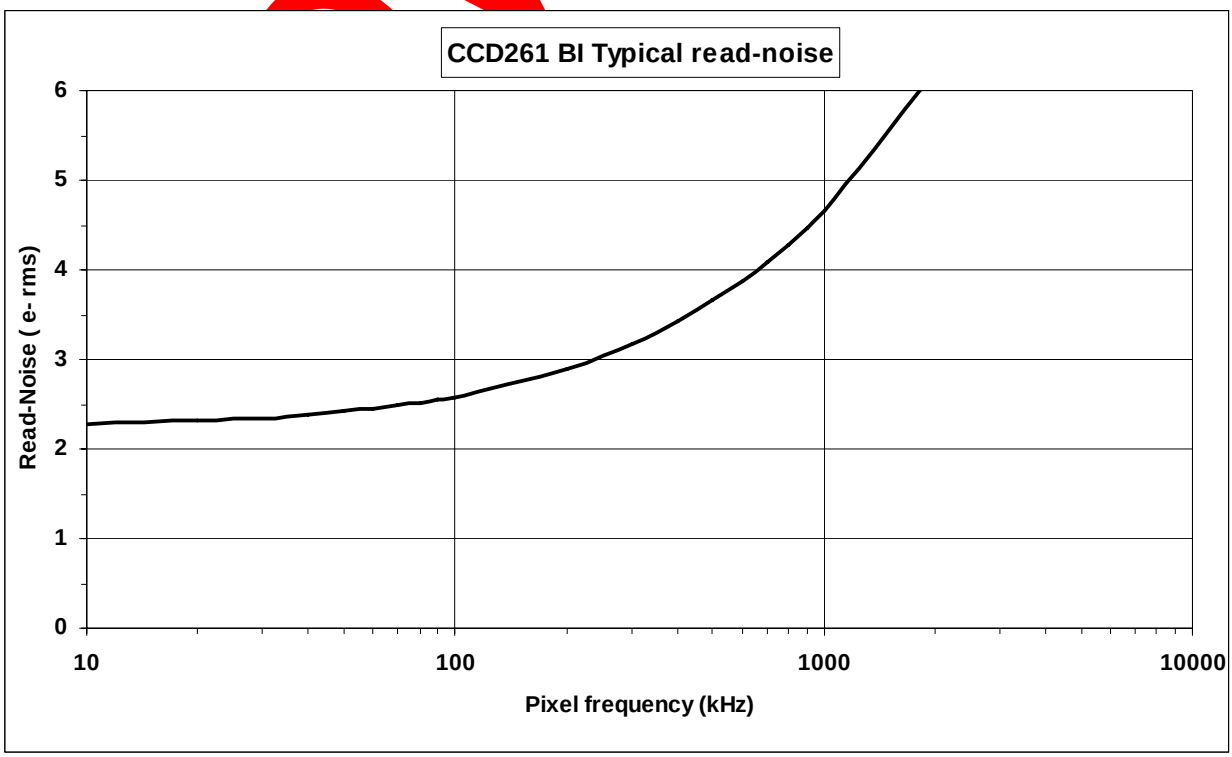
Grade 5 devices are also available. These are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is more than 100 e^- /pixel/hour at 153 K
Black spots	A black spot defect is a pixel with a response less than 50% of the local mean signal.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^- at 153K

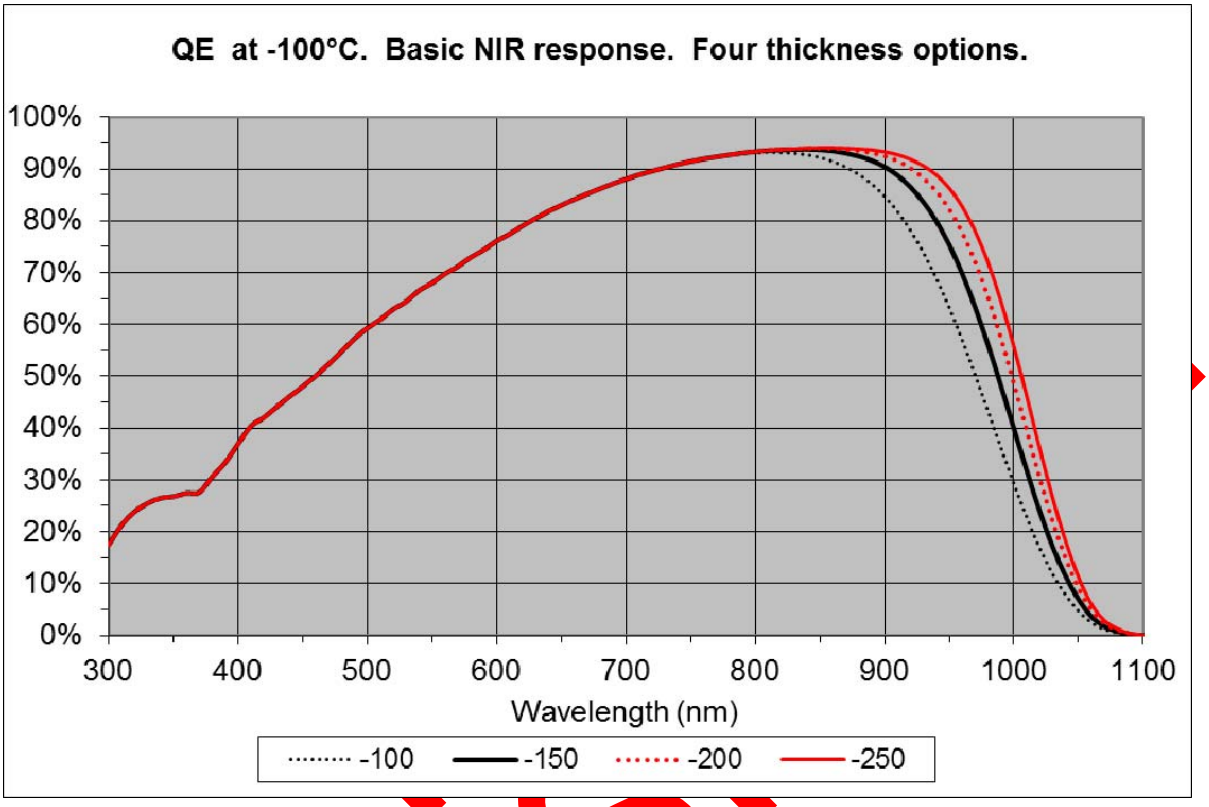
TYPICAL OUTPUT AMPLIFIER NOISE

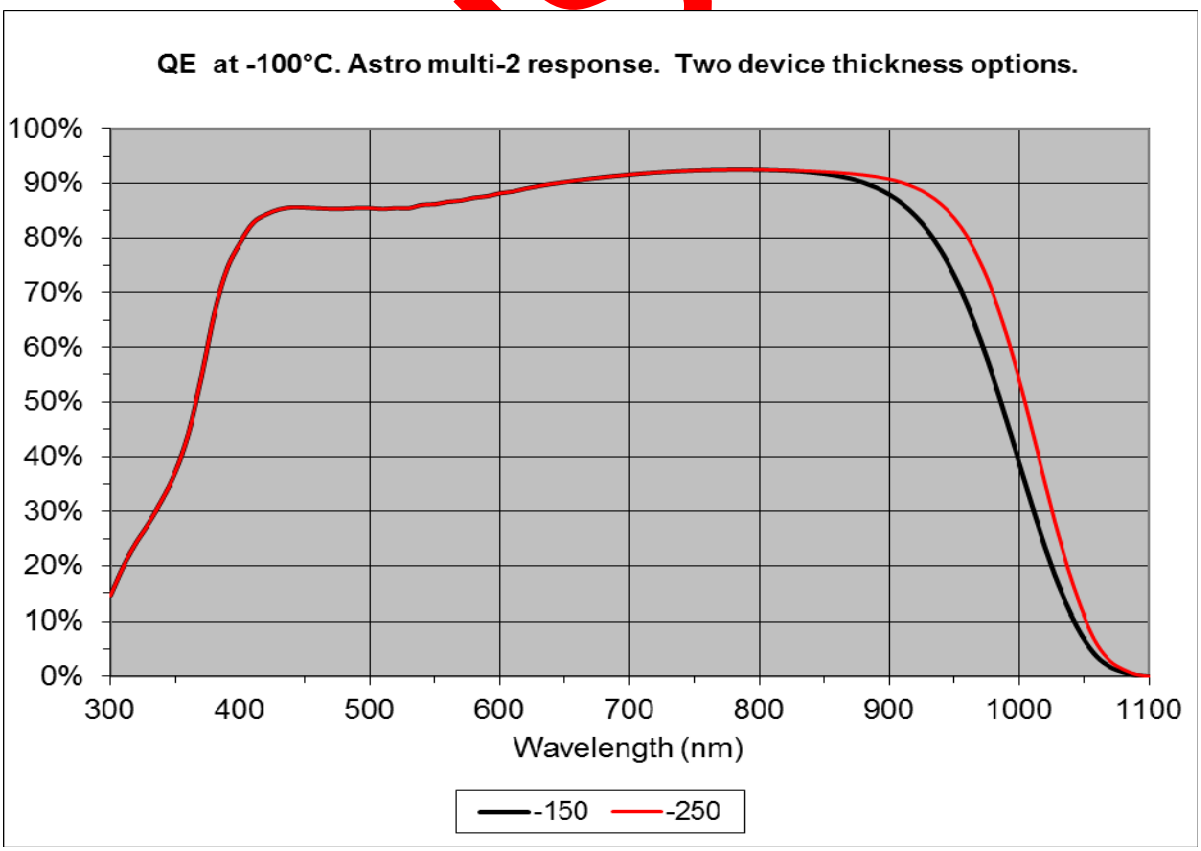
The variation of typical read noise with operating frequency is shown below. [Measured at nominally 153K using correlated double sampling (CDS) with a pre-sampling bandwidth equal to twice the pixel rate].



SPECTRAL RESPONSE

The figures below illustrate high-rho device response for two anti-reflection coatings. Alternate AR coatings can be provided; please consult factory.





The table below gives guaranteed minimum values of the spectral response for several variants

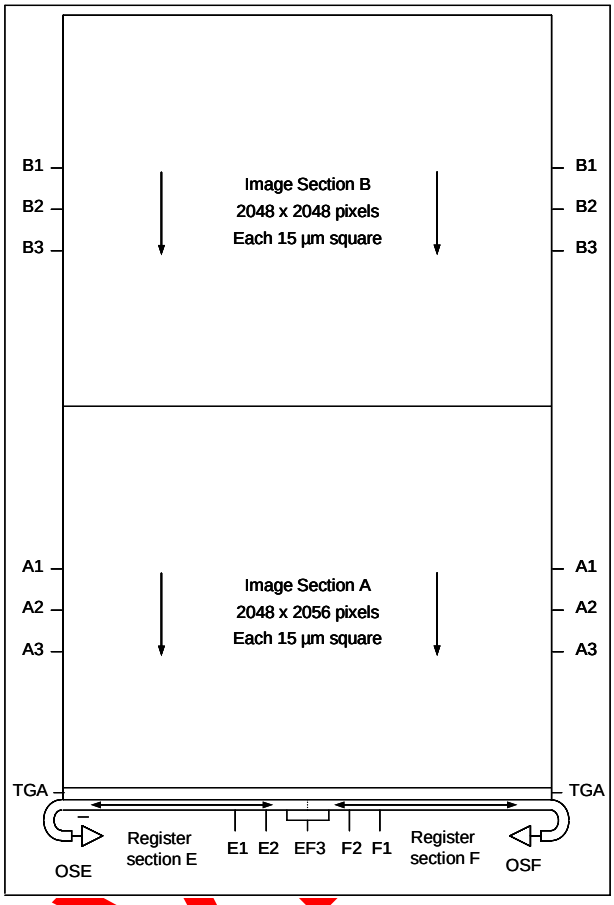
	150 µm Basic NIR	250 µm Basic NIR	150 µm Astro Multi-2	250 µm Astro Multi-2
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**
400	25	25	70	70
500	50	50	75	75
650	75	75	80	80
900	80	85	80	85
1000	30	45	30	45

Use of different thicknesses

The CCD261-84 can be provided with a nominal thickness of 100 µm to 250 µm. The default is 150 µm; others may be provided to custom order.

Increased device thickness provides increased long-wavelength sensitivity, as shown above. This comes at the penalty of increased detection of cosmic rays, which can limit long exposures. In order to attain best point spread function (or MTF) a back bias voltage (VBSS) is required, as discussed later. If this value is too high then some increase in white defects may be seen, and so there can be a trade-off between this effect and that of optimum PSF.

ARCHITECTURE



Device structure looking down onto the photo-sensitive surface

The mask set used for device fabrication can produce numerous variants and these have a common designation for the various features. Thus, in the case of this device, the upper half of the image area is section B and the lower half is section A. The left-hand output and register section is designated E and that on the right is designated F.

The image section drive pulses are designated IØ1, IØ2 and IØ3. Connections are made as follows:

IØ1 = A1 = B1	IØ2 = A2 = B2	IØ3 = A3 = B3

TGA is clocked as IØ3.

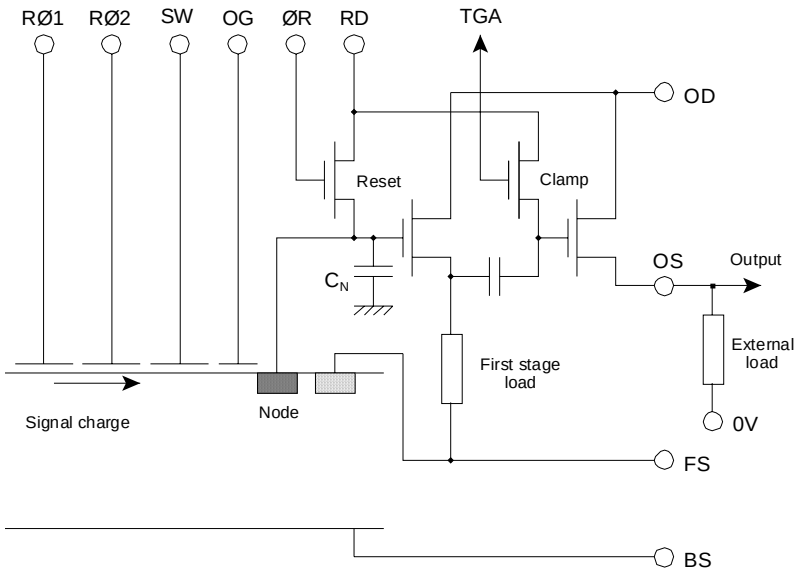
The device is tested and specified in the full-frame mode, but it is also possible to operate in a frame-transfer mode with section B as the image section and section A as the store. Details can be provided on request.

The register drive pulses are designated RØ1, RØ2 and RØ3. Connections are made as follows.

	RØ1	**RØ2**	**RØ3**
E section transfer towards E output	E2	E1	EF3
F section transfer towards F output	F2	F1	EF3
E section transfer towards F output	E1	E2	EF3
F section transfer towards E output	F1	F2	EF3

The summing wells are clocked as RØ3, or held at high level for a number of clock cycles to sum charge.

OUTPUT CIRCUIT (applies to OSE and OSF)



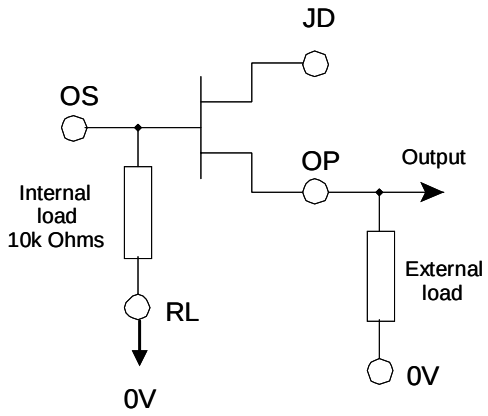
Note. TGA is a device internal connection

The output impedance is typically 400 Ohms.

The on-chip power dissipation is typically 30 mW per amplifier.

If an output is to be powered down, it is recommended that either (a) OD be set to SS voltage, taking care that the maximum ratings are never exceeded or (b) that OD be disconnected. If external loads return to a voltage below SS they should also be disconnected.

Each output has a U309 JFET included within the package for optional buffer use. Both the JFET gate and an internal 10 kΩ load resistor are connected to OS, as shown below. If the output is taken directly from OS with the external load as shown above, then the JFET "floats" and has no function. If the JFET is to be used as a buffer, there is no external load connected to OS but the other ends of the internal loads RL (pins A3/A6) are connected to 0V. The JFET output connections OP (pins B3/B6) each require a constant current load of typically 5 mA, also connected to 0V. The JFET drains JD (pins C3/C6) are biased positively as specified.



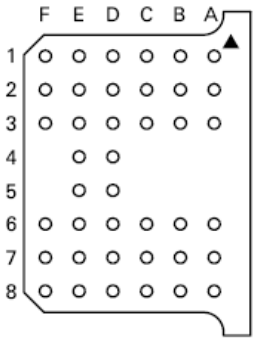
The output impedance is now 100 Ohms and the within-package dissipation is typically 50 mW per amplifier.

ELECTRICAL INTERFACE

The table below give the pin connections and functions

Pin	Name	Function
A1, A8, F2 & F7	FS	Front-substrate
C1 & C8	BS	Back substrate
B2 & B7	GD	Guard drain
E8	B1	Image phase
D8	B2	Image phase
F8	B3	Image phase
D1	A2	Image phase
E1	A1	Image phase
F1	A3	Image phase
F3	TGA	Transfer gate
D3	SWE	Summing well (E)
D2	OGE	Output gate (E)
E3	ØRE	Reset clock (E)
C2	RDE	Reset drain (E)
A2	OSE	Output source (E)
B1	ODE	Output drain (E)
C3	JDE	JFET drain (E)
B3	OPE	JFET output (E)
A3	RLE	JFET load (E)
D4	E1	Serial clock
E4	E2	Serial clock
F6	EF3	Serial clock
E5	F2	Serial clock
D5	F1	Serial clock
D6	SWF	Summing well (F)
D7	OGF	Output gate (F)
C7	RDF	Reset drain (F)
E6	ØRF	Reset clock (F)
B8	ODF	Output drain (F)
A7	OSF	Output source (F)
C6	JDF	JFET drain (F)
B6	OPF	JFET output (F)
A6	RLF	JFET load (F)
E2, E7	-	Reserved

PIN CONNECTIONS (View facing underside of package)



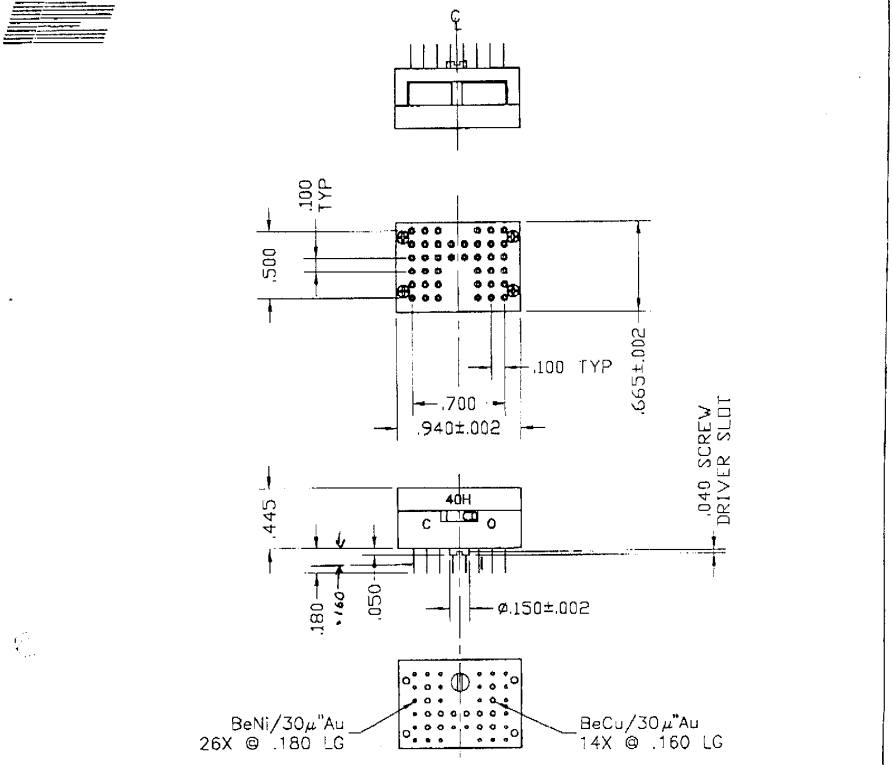
Mating ZIF socket (optional)

web site: www.tacticelectronics.com e-mail: tactic1@airmail.net

Tactic Electronics

ZIF SOCKET 40H

REV.	DATE
B	07/01/00



NOTE: Entry and exit patterns are the same.

Physical
Insulation material: Molded/Machined Torlon and Stainless Steel
Flammability: UL 94V-0
Color: Brown

Contact (.160" lg x .012" x .024"– 14 PLCS)
(.180" lg x .010" x .018"– 26 PLCS)
Material: Beryllium Copper (14X)
Beryllium Nickel (26X)
Plating: 30µ"(.76µm)Gold–MIL–G–45204
Type II,Grade C over 50µ"(1.3µm)
Sulfamate Nickel per QQ–N–290A

Electrical Current Rating: 1 Amp
Insulation Resistance: >1x10⁹Ω at 500Vdc
Withstanding Voltage: 1000 Vrms at Sea Level

Consult factory or your local IACTIC Distributor for design and pricing.
Phone: 1-800-955-4707 FAX: 1-972-702-6135

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OPERATING VOLTAGES

General

The device operates with all primary voltages in the range 0 to +31V, as for other standard e2v CCDs. The front substrate FS is held at 0V, an additional positive bias voltage is required on the guard drain GD, and a negative bias voltage is required on the back substrate BS to fully-deplete the silicon. The front substrate is the primary reference level for most functions.

Note that, unlike most other e2v CCDs, the gate connections are NOT provided with anti-static protection devices. Extreme care should therefore be exercised in handling; details are given later.

Specified values

			Clock or DC Level (V)			Maximum Ratings with respect to FS
Description	**Notes**	**Name**	**Min**	**Typical**	**Max**	
Front substrate voltage	1	FS		0		N/A
Back substrate voltage	2	BS	0	-50 to -70	-100	-100
Guard drain voltage	3	GD	25	30	35	-0.3 to +35
Image sections: clock high level		A/B 1-3	8	12	14	±20
Image sections: clock low level		A/B 1-3	-0.5	0	+0.5	±20
Transfer gate: clock high level		TGA	8	12	14	±20
Transfer gate: clock low level		TGA	-0.5	0	+0.5	±20
Register sections: clock high		E/F 1-3	8	12	14	±20
Register sections: clock low level		E/F 1-3	-0.5	0	+0.5	±20
Output gate		OG	2	3	4	±20
Summing well: clock high level		SWE/SW	8	12	14	±20
Summing well: clock low level		SWE/SW	-0.5	0	+0.5	±20
Reset clock high level		ØRE/	8	12	14	±20
Reset clock low level		ØRE/	-0.5	0	+0.5	±20
Reset drain voltage		RDE/RDF	16	17	18	-0.3 to +35
Output drain voltage		ODE/ODF	27	29	31	-0.3 to +35
Output source voltage	4	OSE/OSF				-0.3 to +35
JFET drain		JDE/JDF		OD + 2		-
JFET source		OPE/OPF				-
Source load for JFET input	5	RLE/RLF		0		-

Notes

1) Reference level for all voltages

2) Adjust to achieve full depletion. Ensure it is equal to FSS at power-up; see power-up/down in next section. A specific recommended value will be provided on the test sheet to be delivered with science-grade devices.

3) May need to be adjusted in conjunction with BS voltage to minimise leakage currents. The default value is expected to be 30V. Any alternate recommended value will be shown on the device test sheet.

4) See details of output circuit. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is typically 5V more positive than that on RD. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS experiences short circuit conditions.

For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

5) Connect to 0V only if the JFET is in use.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

Connection	Typical
A-A and B-B inter-phase	22 nF
A-SS & B-SS	10 nF
TGA	35 pF
E1 & F1 total load	65 pF
E2 & F2 total load	65 pF
EF3 total load	100 pF
∅R-SS	20 pF

Electrode series resistance

Section	Typical
A	30 Ω
B	50 Ω
E1, E2, F1 & F2	10 Ω
EF3	6 Ω

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. This includes ensuring that reverse bias voltages cannot be momentarily applied.

The CCD has 2 substrates. The front substrate FS for the output circuit is set to 0V. The back substrate BS is applied to the back surface of the CCD. To get full depletion a large negative potential is applied. A guard drain is designed to isolate front and back substrates.

If there is a current flowing between FS and BS when switching on the guard drain, the insulation below the guard ring might not form properly. It is therefore advised to first set both FS and BS to 0V, then switch on the guard drain and all other biases and clocks in the conventional order, before applying any negative bias to BS. The recommended power up order of all biases and clocks is listed in the table below.

BIAS/CLOCK	LABEL	POWER UP ORDER	Comment
Front Substrate	FS	1	**Reference voltage 0V**
Back Substrate	BS	1	**Set to 0V at this stage**
Guard Drain	GD	2	
Reset Drain	RD	2	
Output Drain	OD	2	
Output Gate	OG	3	
Image Clock High	IØH	4	
Image Clock Low	IØL	4	
Register Clock High	RØH	4	
Register Clock Low	RØL	4	
Reset Gate High	ØRH	4	
Reset Gate Low	ØRL	4	
Back Substrate	BS	5	**Set to desired voltage**

It is also important to ensure that excess currents do not flow in the OS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

POWER CONSUMPTION

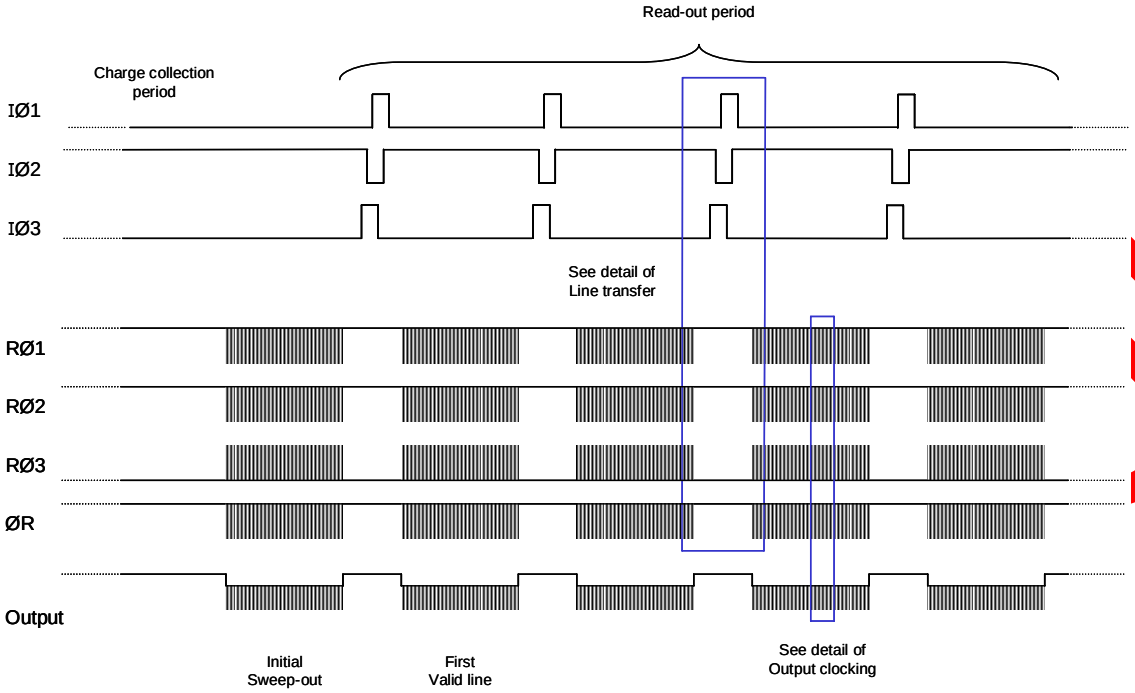
The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives representative values for the components of the on-chip power dissipation for the case of a full-frame device with continuous line-by-line read-out using one amplifier (but with both on-chip amplifiers powered-up). The frequency is that for clocking the serial register. There will be additional dissipation if the JFET amplifiers are used.

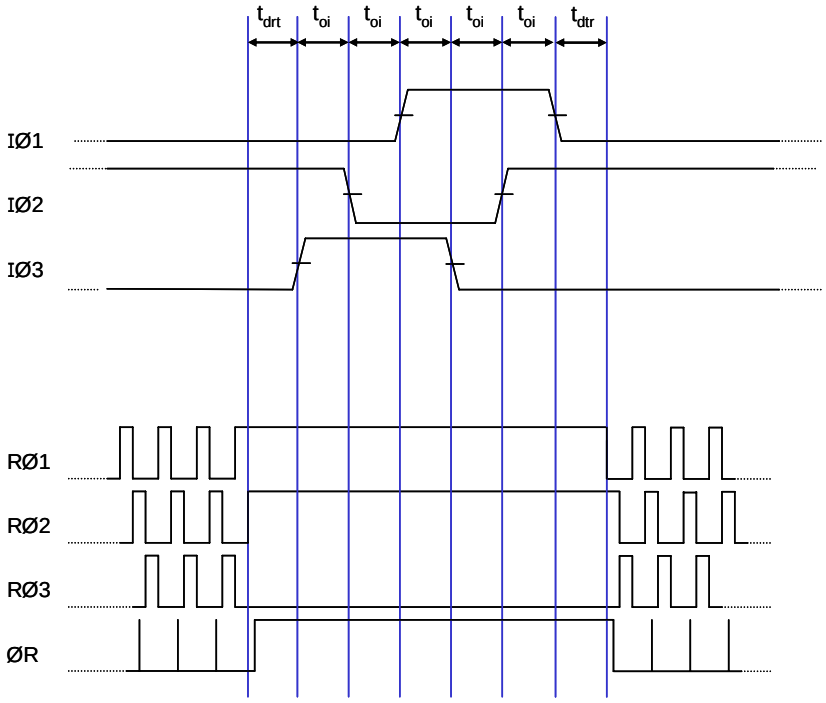
Readout frequency	Line time	Power dissipation			
		Amplifiers	Serial clocks	Parallel clocks	Total
20 kHz	100 ms	60 mW	< 1 mW	< 1 mW	61 mW
100 kHz	20 ms	60 mW	2 mW	1 mW	63 mW
1 MHz	2 ms	60 mW	23 mW	13 mW	96 mW

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

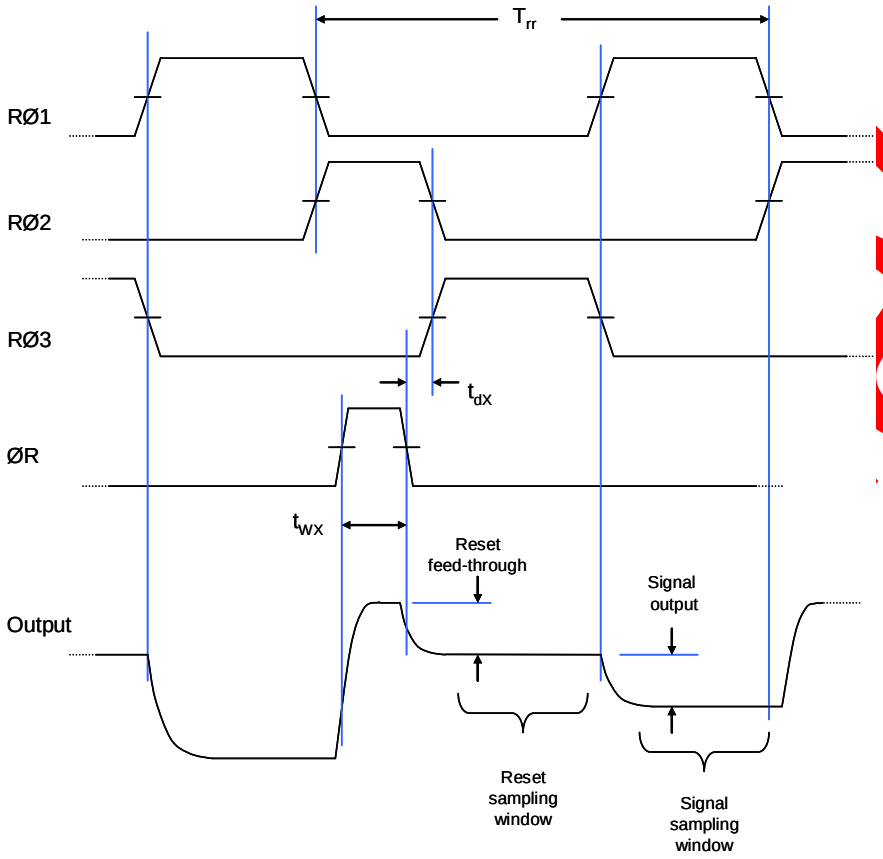
FRAME READOUT TIMING DIAGRAM



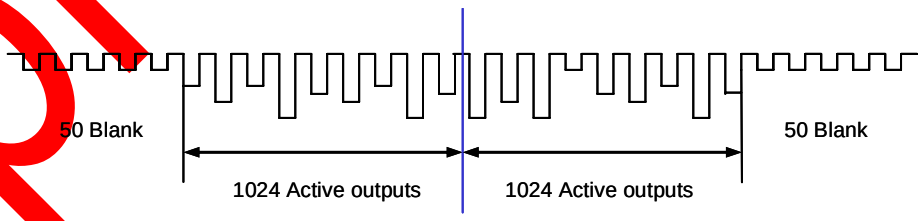
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT

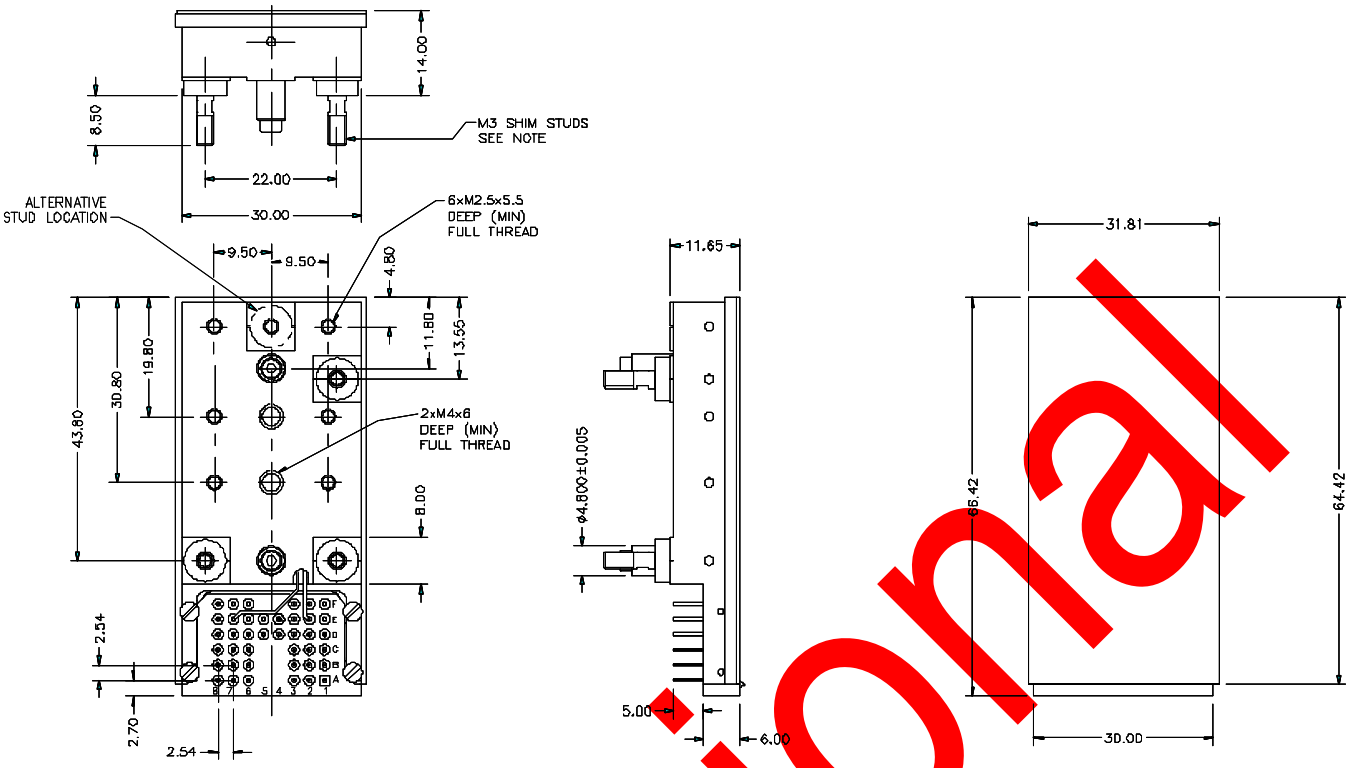


CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
t_{oi}	Image clock pulse overlap	10			µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	0.2 t_{oi}		µs
t_{fi}	Image clock pulse fall time (10 to 90%)	1	0.2 t_{oi}		µs
t_{dir}	Delay time, IØ stop to RØ start [note 1]	10	500		µs
t_{dri}	Delay time, RØ stop to IØ start	1			µs
T_r	Output register clock cycle period	1	50		µs
t_{rr}	Register pulse rise time (10 to 90%)		0.1T_r	0.2T_r	ns
t_{fr}	Register pulse fall time (10 to 90%)		0.1T_r	0.2T_r	ns
t_{or}	Register pulse overlap (50%)	0	10	0.1T_r	ns
t_{wx}	Reset pulse width		0.2 T_r		ns
t_{rx}	Reset pulse rise and fall times		10		ns
t_{dx}	Delay time, ØR low to RØ3 low	0	10		ns

Note 1. Ensure adequate settling after image triplet before initiating register readout

PACKAGE DETAIL



Note
The device is supplied with shim studs to hold it onto the mounting plate; these are fitted to three of the four holes. The default unless specified is the third stud in the offset position. An optional stud of length 15.0 mm can be supplied if requested at time of order.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Unlike most e2v devices, the CCD261 is NOT provided with anti-static protection devices on the gate connections. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty.

The devices are assembled in a clean room environment and e2v technologies recommend that similar precautions are taken by the user to avoid contaminating the active surface.

The compact buttable package allows a good fill factor in close-butted mosaics, but requires careful handling to avoid device damage. Consult factory for advice if required.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range	153 - 323 K
Storage temperature range	73 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 153 K.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.

MATING CONNECTOR

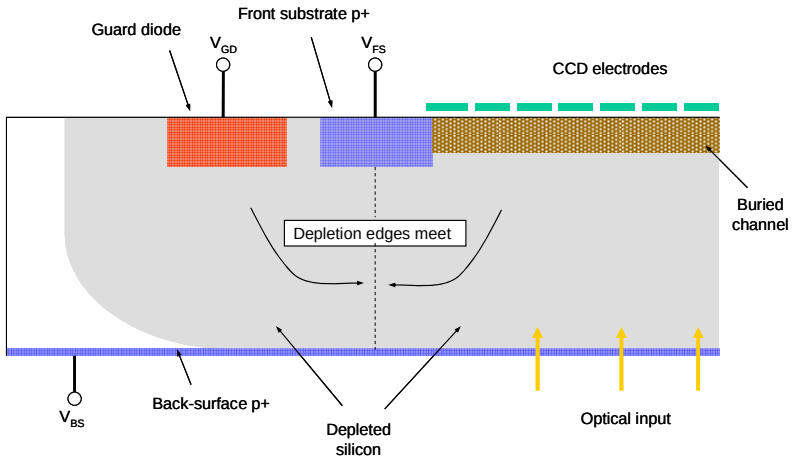
A custom ZIF connector is available for use with this sensor. The ZIF socket fits within the footprint of the package to optimise close-packing of mosaic assemblies. Contact e2v technologies for details.

Hi-Rho Device Technology

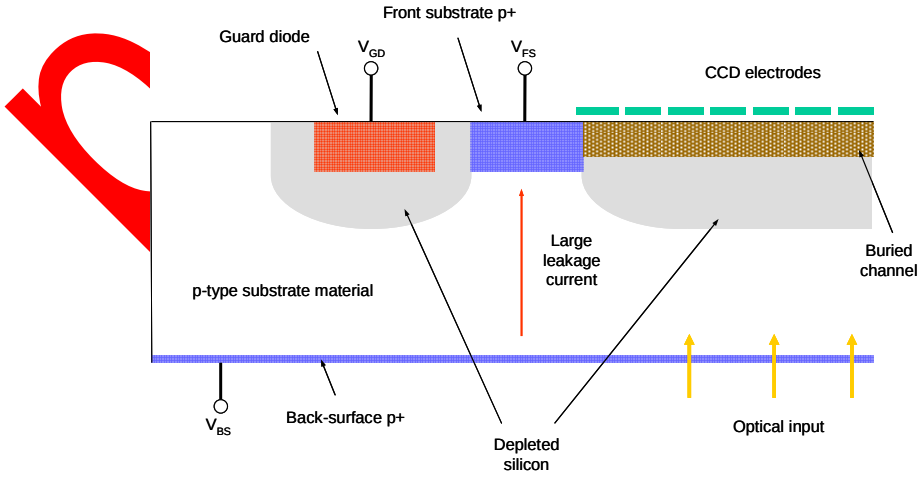
Extending the long wavelength response of back-face devices requires the use of thicker silicon, but this must be fully depleted to avoid loss of spatial resolution through sideways diffusion of charge. The depth of depletion is proportional to square root of the operating voltages and the silicon resistivity, but there is a practical limit to both and possibilities for maintaining full-depletion with increasing thickness are therefore limited. The new Hi-Rho technology is a way of overcoming this limitation.

In standard devices the bulk of the silicon substrate is all at the same bias voltage V_{SS}. It is possible to take V_{SS} to negative voltages to increase depletion, but the limit is generally set by the onset of avalanche breakdown in the p-n junctions of the output circuit components.

The Hi-Rho technology allows the use of a larger negative substrate bias on the back of the silicon V_{BS} to increase the depth of depletion under the electrodes, whilst still maintaining a bias on the front-surface of the silicon V_{FS} at a voltage level normally used for V_{SS} such that the output circuits function normally. However, for this to be possible, current flow between the front and back bias connections must be avoided. This is achieved using an additional “guard diode” at bias V_{GD}, as shown below.



With correct bias conditions the depletion regions from the CCD channel and the guard diode merge to block the conductive path, rather like the operation of a JFET, as shown above. If incorrect, then there is a direct resistive path between the front and back contacts and excessive currents can flow, as shown below.



It is therefore important to use the specified bias levels and the switch-on and switch-off sequences.